Single Cycle Read/Write/WriteBack Pipeline, Full-Wordline I/O DRAM Architecture with Enhanced Write and Single Ended Sensing

ABSTRACT OF THE INVENTION

A DRAM is disclosed which includes a single ended bitline structure, a single ended global bitline structure, primary sense amplifiers with data storage and data write-back capability and with capability to decouple from the global bitlines, a full-wordline I/O structure where essentially all memory cell that belong to the same wordline are being operated on, and a pipelined architecture. The DRAM further includes a small voltage swing design. The primary sense amplifiers can include more than one amplification stages. Such a DRAM is suitable for applications in conjunction with processors as an embedded DRAM.